CLAIMS

What is claimed is:

1. A method to facilitate evaluating an integrated circuit (IC) chip comprising:

determining a set of critical paths for a design associated with the IC chip, at least some of the critical paths being determined based on timing characteristics thereof;

generating a plurality of sets of timing test patterns for the set of critical paths, each set being generated according to desired performance criteria; and

applying at least one of the plurality of sets of test patterns to the IC chip to provide corresponding test data indicative of performance-related characteristics of the IC chip.

2. The method of claim 1, the timing characteristics including a timing threshold indicative of slack between endpoints of an associated path of the design associated with the IC chip, the set of critical paths including data paths of the design associated with the IC chip having a slack less than that defined by the timing threshold.

3. The method of claim 1, the determination of the set of critical paths further comprising performing static timing analysis on the design associated with the IC chip to provide slack characteristics for paths of the design associated with the IC chip.

4. The method of claim 3, the determination of the set of critical paths further comprising:

defining the timing characteristics as a slack limit; and

identifying the critical paths of the design associated with the IC chip based on a comparison of the slack limit relative to the slack characteristics provided by the static timing analysis for paths of the design associated with the IC chip.

5. The method of claim 1, the desired performance criteria of each set of the test patterns further comprising a target speed related characteristic.

6. The method of claim 1, further comprising grading a performance characteristic of the IC chip based on the test data for at least one set of the plurality of sets of test patterns.

7. The method of claim 1, the application of the at least one of the plurality of sets of test patterns further comprising:

applying a first set of the plurality of test patterns to the IC chip, the desired performance criteria associated with the first set of test patterns defining a first associated performance level for the IC chip; and

ascertaining whether the IC chip meets the first associated performance level based on the corresponding test data.

8. The method of claim 7, the application of the plurality of sets of test patterns further comprising:

if the IC chip fails the first associated performance criteria, applying at least one other set of the plurality of sets of test patterns to the IC chip, the desired performance criteria associated with the at least one other set of test patterns defining a second associated performance level for the IC chip; and

ascertaining whether the IC chip meets the second associated performance level based on the corresponding test data.

9. The method of claim 1, further comprising applying a stress to the IC chip at least one of before or after the application of the at least one of the plurality of sets of test patterns.

10. The method of claim 9, further comprising determining an impact on performance of the IC chip associated with the application of stress to the IC chip.

11. The method of claim 10, the determination of the impact on performance of the IC chip further comprising determining an impact on speed degradation of the IC chip associated with the application of stress to the IC chip.

12. The method of claim 10, the determination of the impact on performance of the IC chip further comprising identifying a location on the IC chip impacted by the application of stress to the IC chip and at least one potential process parameter capable of causing a defect at the location during fabrication of the IC chip.

13. The method of claim 1, further comprising:

evaluating the test data for the plurality of sets of test patterns to ascertain an indication of process variations associated with the fabrication of the IC chip; and

employing the indication of process variations to adjust process parameters for subsequent fabrication of IC chips based on the design associated with the IC chip.

14. The method of claim 1, further comprising evaluating the test data generated for each set of the plurality timing patterns to identify performance capabilities of the IC chip.

15. A computer-implemented method to determine performance-related characteristics of an integrated circuit (IC) chip, the method comprising:

applying a first set of test patterns of a plurality of sets of test patterns to the IC chip, the plurality of test patterns being generated for a subset of critical paths of the IC chip based on timing characteristics of the subset of critical paths ascertained from timing analysis of a design for the IC chip;

storing test data based on the application of the first set of test patterns;

repeating the application and the storing for each other set of test patterns of the plurality of test patterns; and

evaluating the stored test data for the IC chip for at least one of the plurality of sets of test patterns to provide an indication of at least one of performance-related characteristic of the IC chip.

16. The method of claim 15, the timing characteristics is a timing threshold indicative of slack between endpoints of an associated path of the design of the IC chip, the subset

of critical paths including data paths having a slack less than that defined by the timing threshold.

17. The method of claim 15, each set of plurality of sets of test patterns further being generated for a target operating speed related characteristic.

18. The method of claim 15, further comprising grading a performance characteristic of the IC chip based on the stored test data for at least one set of the plurality of sets of test patterns.

19. The method of claim 15, further comprising applying a stress to the IC chip before application of at least one the first set and the other sets of test patterns.

20. The method of claim 19, further comprising determining an impact on performance of the IC chip associated with the application of stress to the IC chip.

21. The method of claim 20, the determination of the impact on performance of the IC chip further comprising determining an impact on speed degradation of the IC chip associated with the application of stress to the IC chip.

22. The method of claim 20, the determination of the impact on performance of the IC chip further comprising identifying a location on the IC chip impacted by the application of stress to the IC chip and at least one potential process parameter capable of causing a defect at the location during fabrication of the IC chip related to the impact on performance of the IC chip.

23. The method of claim 15, further comprising:

the evaluation of the stored test data further comprising evaluating the stored test to ascertain an indication of process variations associated with the fabrication of the IC chip; and

employing the indication of process variations to adjust process parameters for subsequent fabrication of IC chips based on the design of the IC chip.

24. A system to facilitate evaluating performance of an integrated circuit chip, comprising:

means for identifying a set of critical paths of the IC chip based on timing margins associated with at least some paths of the set of critical paths ;

means for generating test patterns for the set of critical paths of the IC chip based on a plurality of target performance criteria; and

means for applying the test patterns to the IC chip to generate test data indicative of performance for the IC chip.

25. The system of claim 24, further comprising means for defining different desired target performance criteria for each of a plurality of sets of test patterns.

26. The system of claim 24, further comprising:

means for applying stress to the IC chip; and

means for evaluating an impact the stress has on performance of the IC chip.

27. The system of claim 24, further comprising means for ascertaining an indication of process variations associated with fabrication of the IC chip based on the test data.

28. The system of claim 24, further comprising means for ascertaining an indication of operating speed performance associated with fabrication of the IC chip based on the test data.